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~~Sequential Circuits How~~

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~~Example 70: Block RAM~~

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VHDL program. library  
IEEE; use IEEE.STD\_LOGIC\_1164.ALL;

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Verify...

VHDL Tutorial – 12:

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Introduction to Logic  
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This chapter explains the  
VHDL programming for  
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VHDL Code for a Half-  
Adder VHDL Code:

```
Library ieee; use  
ieee.std_logic_1164.all;  
entity half_adder is  
port(a,b:in bit;  
sum,carry:out bit); end  
half_adder; architecture
```

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```
data of half_adder is  
begin sum<= a xor b;  
carry <= a and b; end  
data;
```

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Verilog. Both languages are used for hardware design, so there are a number of books that focus on underlying design and engineering concepts and use both VHDL and Verilog.

Digital Design with RTL Design, VHDL, and Verilog

Get Started with VHDL Programming: Design

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Your Own ...

This chapter explains  
how to do VHDL  
programming for  
Sequential Circuits.

```
VHDL Code for an SR  
Latch  
library ieee; use  
ieee.std_logic_1164.all;  
entity srl is port(r,s:in bit;  
q,qbar:buffer bit); end srl;  
architecture virat of srl is  
signal s1,r1:bit; begin  
q<= s nand qbar; qbar<=  
r nand q; end virat;
```

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